Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 50035

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – JAN. 2026
Fourth Semester
Computer Science and Engineering
U19CS410 – COMPUTER ORGANIZATION
(Regulation 2019)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Write down the CPU performance equation that is used to calculate execution time. Brief about its parameters.	2	K1	CO1
2.	Tabulate the cardinal differences between RISC and CISC architectures.	2	K2	CO1
3.	Why is the "Wait for MFC" step necessary when performing read or write operations to the main memory?	2	K2	CO2
4.	List down typical addressing modes supported by small processors.	2	K1	CO2
5.	Enumerate and explain the four key stages involved in instruction pipelining.	2	K1	CO3
6.	Define the following terms in the context of instruction execution(IR). • Branch taken • Branch target	2	K1	CO3
7.	State the importance of cache memory with respect to overall processor performance.	2	K1	CO4
8.	A program running on a computer with a cache performs 1400 instruction fetches from the cache and 100 instruction fetches from main memory. What is the cache hit rate?	2	K2	CO4
9.	List the difference between asynchronous Bus and synchronous Bus.	2	K2	CO5
10.	What are the various types of Controllers connected to the SCSI Bus?	2	K1	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Explain the addressing modes for the modern processors, and how the Effective address or Offset is determined by adding any combination of three address elements.	13	K2	CO1
		(OR)			
	b)	Explain in detail about instruction sequencing, including aspects such as instruction length and pipeline execution patterns.	13	K2	CO1
12.	a)	Sketch and explain the single bus organization of the data path inside a processor.	13	K2	CO2
		(OR)			
	b)	Sketch and explain the multiple bus organization in detail. What are the Benefits of using Multiple-Bus Architecture compared to Single-Bus Architecture?	13	K2	CO2
13.	a)	Explicate Data Hazards which causes to stall. Illustrate how to reduce or eliminate the occurring of data hazard.	13	K2	CO3
		(OR)			
	b)	The time delay for four segments in pipeline are as follows: t1=50ns, t2=30ns, t3=95ns and t4=45ns. The interface register delay time tr=5ns. How long would it take to add 100 pairs of numbers in the pipeline and how can we reduce the total time to about one half of the time calculated.	13	K3	CO3
14.	a)	Examine the cache memory organization and the various techniques for improving cache performance in detail.	13	K3	CO4
		(OR)			
	b)	A processor with a 1ns clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Calculate Memory Access Time (MAT). Assume that the read and write miss penalties are the same and ignore other write stalls.	13	K2	CO4
15.	a)	Explain the types of Interface circuits available in Input /Output Organization.	13	K2	CO5
		(OR)			
	b)	Paraphrase about Programmed Input and Output concepts in detail.	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate i. Pipeline cycle time. ii. Non-pipeline execution time. iii. Speed up ratio. iv. Pipeline time for 1000 tasks. v. Sequential time for 1000 tasks. vi. Throughput.	15	K3	CO3
		(OR)			
	b)	Scenario: A technology company is designing a new processor architecture for mobile devices. The architecture aims to optimize power efficiency while maintaining high performance for a wide range of applications. The company's design team has proposed a novel approach for instruction scheduling in the processor pipeline. Task: Assuming the proposed instruction scheduling mechanism involves a speculative execution strategy, analyze the potential advantages and disadvantages of this approach in terms of power efficiency and performance. Provide specific examples and justifications to support your analysis.	15	K4	CO4